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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/759,940	01/16/2004	David William Boerstler	AUS920030715US1	8206

7590 03/16/2005

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EXAMINER	
TRA, ANH QUAN	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 03/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/759,940	BOERSTLER ET AL.	
	Examiner	Art Unit	
	Quan Tra	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

The specification is objected because the recitation in page 11, lines 21-24, is not enable. page 11, lines 21-24 recites that "The width (W) and length (L) of the current mirror 350 is varied such that the voltage across the second capacitor 316 is substantially equal to the voltage across the first capacitor 304". However, Kirchhoff's voltage law teaches that sum of voltages in a close loop is equal to zero. Therefore, the voltage across applicant's capacitor 304 is equal to the voltage across capacitor 316 add (+) the voltage across transistor 318. In order for the voltage across capacitor 316 to be equal to the voltage across capacitor 304, the voltage across transistor 318 must be equal to zero Volt. It is not seen how the width and length of transistor 318 are adjusted in order to make the voltage across transistor 318 to be zero volt.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-11 and 16-26 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claims 1 and 16 recite that "at least one current mirror is at least configured be coupled the scaled capacitor that

at least configured to provide a potential difference across the scaled capacitor that substantially equal potential difference across the leaky capacitor". However, according to Kirchhoff's voltage law, in order to make the voltage across capacitor 316 to be equal to the voltage across capacitor 304, the voltage across transistor 318 must be equal to zero voltage. It is not seen how the width and length of transistor 318 are adjusted in order to make the voltage across transistor 318 to be zero volt.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 14 and 15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 14 and 15 are misdescriptive and rendered the claims indefinite. It is misdesctitive to recite "a computer code for ...". However, figure 3 of the application shown only circuitry, no software is used.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Drusenthal (USP 6806749) in view of Alvarez (Fundamental Circuit Analysis, printed by Science Research Associtates, Inc, 1978, pages 378-379).

As to claim 1, Drusenthal's figure 5 shows a capacitor C2 coupled to plurality of current mirrors (SE1, SE2). Figure 5 fails to shows plurality of capacitor of different sizes coupled to the plurality of current mirrors. However, Alvarez teaches in pages 378-379 that a capacitor can be made by a plurality of parallel connected capacitors having different sizes in order to meet a desire capacitance. Therefore, it would have been obvious to one having ordinary skill in the art to use plurality of parallel connected capacitors having different sizes for Drusenthal's capacitor C2 due to doctrine equivalent function and in order to meet a particular desire capacitance for capacitor C2. Thus, the largest capacitor in the combination of parallel connected capacitors C2 anticipates the claimed Leaky capacitor, and the smallest capacitor in the combination of parallel connected capacitors C2 anticipates the claimed scale capacitor. The modified Drusenthal's figure 5 shows: an apparatus for current leakage correction coupled to a leaky capacitor (the largest capacitor in the parallel connected capacitors C2), comprising: a scaled capacitor (the smallest capacitor in the parallel connected capacitors C2), wherein the scaled capacitor has an area reduced by a scaling factor in comparison to the leaky capacitor; and a plurality current mirrors (SE1, SE2), wherein the plurality of current mirrors further comprise: at least one current mirror (SE1) is at least configured to be coupled to the leaky capacitor; and at least one current mirror (SE2) is at least configured to be coupled to the scaled capacitor that at least configured to provide potential difference across the scaled capacitor that is substantially equal to a potential difference across the leaky capacitor.

As to claim 2, the modified Drusenthal's figure 5 shows that the plurality of current mirror further comprises a plurality of transistors.

As to claim 3, the modified Drusenthal's figure 5 shows that the plurality of current mirrors further comprises a plurality of Field Effect Transistors (FET).

As to claim 4, the modified Drusenthal's figure 5 shows that at least one FET (T4, T5) of the plurality of FETS is a Positive-channel FET (PFET), the PFET is at least configured to inject current into the leaky capacitor to compensate for a current leak.

As to claims 5 and 6, the modified Drusenthal's figure 5 shows that at least one FET (T1, T2) of the plurality of FETS is a Negative-channel FET (NFET).

As to claim 7, Drusenthal's column 8, lines 20-22, teaches that the plurality of current mirrors further comprise a plurality of bipolar transistors.

As to claim 8, the modified Drusenthal's figure 5 shows that the plurality of current mirrors further comprise a plurality of Metal-oxide Semiconductor FETS (MOSFETS).

As to claim 9, the modified Drusenthal's figure 5 shows that at least one MOSFET of the plurality MOSFETS is a Positive-type MOSFET (P-type MOSFET), the P-type MOSFET is at least configured to inject current into the leaky capacitor to compensate for a current leak.

As to claims 10 and 11, the modified Drusenthal's figure 5 shows that at least one FET of the plurality of FETS is a Negative-type MOSFET (N-type MOSFET).

As to claim 12, the modified Drusenthal's figure 5 shows a method for current leakage correction for a leaky capacitor (the largest capacitor in the parallel connected capacitors C2), comprising: measuring (by SE1) voltage across the leaky capacitor; providing the measured voltage a scaled capacitor (the smallest capacitor in the parallel connected capacitors C2),

wherein the scaled capacitor has an area reduced by a scaling factor in comparison to the leaky capacitor; and providing a sustaining charge to the leaky capacitor.

As to claim 13, the modified Drusenthal's figure 5 shows the step of providing the measured voltage to a scaled capacitor further comprises utilizing plurality of current mirrors (SE1, SE2) with an adjusted width and length to provide the measured voltage to the scaled capacitor.

Claims 14 and 15 recite similar limitations of claims 12 and 13. Therefore, they are rejected for the same reasons.

Claims 16-26 recite similar limitations of claims 1-11. Therefore, they are rejected for the same reasons.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 571-272-1755. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

March 9, 2005

QUAN TRA
PRIMARY EXAMINER